REMARKS

Reconsideration of the present application is respectfully requested. As this response is submitted pursuant to 37 C.F.R. §1.116, entry is respectfully requested. It is submitted that the present paper does not raise new issues for consideration or new grounds for search, and therefore, entry is proper here. Claims 1-14 are pending herein, with claims 9-14 previously withdrawn from consideration in response to a restriction requirement. Thus claims 1-8 and 15 are under consideration at the present time.

Claims 1-5, 7, 8 and 15 stand rejected under 35 U.S.C. §102(b) as anticipated by Kepler et al., U.S. Patent No. 6,100,145. According to the examiner, Kepler et al. teaches a method of fabricating a semiconductor device, comprising, *inter alia*, a second step (b) in which a first thermal annealing is *inherently provided* to the substrate. According to the examiner, this step is inherently practiced to the source/drain regions of the device.

The applicants respectfully disagree with the examiner's "inherency" contention concerning the first thermal annealing. The examiner implicitly recognizes that Kepler et al. does not teach annealing subsequent to applying a non-conductive oxide film, and thus he must contend the annealing step is inherent. It is incumbent upon the examiner to do more than make bald assertion of inherency, as has occurred here. Under U.S. law, the examiner must, in making out a *prima facie* case of non-patentability, demonstrate that the reference in question more likely than not teaches what is claimed in the application under consideration. Here, the examiner must provide evidence supporting the contention of inherency. As set forth in §2112 of the Manual of Patent Examining Procedure,

> "The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert,* 9 F.3d 1531, 28 USPQ2d 1955, 1957 (Fed. Cir.

> 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich,* 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). 'To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' ' *In re Robertson,* 169 F.3d 743, 745, 49 USPQ2d 1949, 150-51 (Fed. Cir. 1999) (citations omitted)
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> In replying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.' *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

The examiner has done no more than assert that annealing of the substrate "for forming the source/drain regions". No evidence supports this assertion. Furthermore, as the applicants noted in their prior response, there is a difference in the timing of the annealing step between the prior art teachings and the claimed process, and therefore, it appears that an annealing step is not inherent in Kepler at the required time.

Specifically, as indicated in the applicants' previous response, the present specification shows that formation of the source/drain regions 108 take place prior to depositing the oxide film, as disclosed in the present specification at page 2, line 9, page 4, lines 4-6, and page 9, lines 6-9. Furthermore, Kepler et al. itself is consistent on this point, as Kepler et al. specifically states at col. 4, lines 1-4 that

> According to the methodology of the present invention, a buffer layer of silicon is blanket deposited on a substrate after forming the source/drain implants, i.e., on source/drain regions and also on field oxide regions, gates and spacers.

Thus, if the examiner's rationale were correct, it appears that annealing would "implicitly" occur in Kepler et al's process earlier than as contended in the office action, as the formation of source/drain regions takes place prior to fabrication of the substrate. Thus, it should

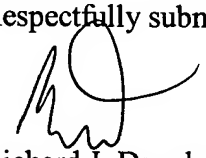
be evident, with source drain regions formed earlier in both Kepler et al's disclosure and in the disclosure of the present process, that there is no basis whatsoever for the examiner to contend that it is inherent in Kepler et al. to practice a first thermal annealing, after oxide film formation over the semiconductor substrate, as set forth in claim 1. For this reason, it is the applicant's position that the first thermal annealing after oxide layer formation is not necessarily present in Kepler et al.

Furthermore, the reference does not teach an annealing step subsequent to depositing of the metal layer.

Also, claim 6 is rejected under 35 U.S.C. §103(a) as unpatentable over Kepler et al. in view of Huang and Jeng. These references do not cure the deficiencies with respect to the Kepler reference.

Wherefore, based upon the foregoing, it is respectfully submitted that the present application is in condition of allowance and a relatively early reply is requested.

Respectfully submitted,



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